REMARKS

In response to the Official Action mailed on November 29, 2006:

[1-2] Claims 1, 4, and 5 were rejected under §102(e) as being anticipated by Sugerman '840. This rejection is respectfully traversed. New claim 32, with notations to examples of its subject matter in the disclosure, recites

A semiconductor apparatus [Figs. 1-3] *comprising:*

an output electrode [12] *from which an output signal of the semiconductor apparatus is output;*

a first-conductivity-type MOS output transistor [11] *respectively including a drain electrode* [upper terminal in Fig. 1(a); 25 in Fig. 1(b)] *connected to the output electrode* [12], *a source electrode* [26] *connected to a ground voltage terminal* [13], *a gate electrode* [21] *connected to a signal line* [24], *and a second-conductivity-type layer* [22 in Fig. 1(b)] *located under the gate electrode* [21], *wherein the first-conductivity-type MOS output transistor transmits the output signal of the semiconductor apparatus to the output electrode responsive to a signal on the signal line* [24];

a first-conductivity-type MOS protection transistor [10] *respectively including a drain electrode* [upper terminal in Fig. 1(a); 15 in Fig. 1(b)] *connected to the output electrode* [12], *a source electrode* [lower terminal in Fig. 1(a); 16] *connected to the ground voltage terminal* [13], *and a gate electrode* [heavy vertical line in Fig. 1(a); 14 in Fig. 1(a)] *connected to the ground voltage terminal* [13]; *and*

a metallic wiring member [28, amended Fig. 1(b)] *which connects the second-conductivity-type layer* [22] *of the first-conductivity-type MOS output transistor to the gate electrode* [14] *of the first-conductivity-type MOS protection transistor* [10].

The advantage of the metallic wiring member is explained at page 10, line 28: "The layout view of FIG. 2 shows ... gate electrode 14 of the NMOS dummy transistor 10 is connected to the P+

contact layer 27 (P-well 22) .... the gate electrode 14 is connected to a metal wiring 28 connected to the P-well 22. Because the gate electrode 14 and the P-well 22 are connected by the electrode wiring, the layout area does not increase compared with the conventional structure."

Sugerman does not disclose several features of the new claim.

(1) Sugerman does not disclose a device with an input and an output. It discloses two bus bars 20 and 30 held at different voltages, which power an non-specific device 10 (Fig. 4 and col. 5, lines 45). The transistors m10 and m11 are intended solely for electrostatic discharge and they have no signal input or signal output. Therefore, they do not anticipate the claimed apparatus which accepts a signal coming in on signal line (exemplified by 24 in Fig. 1(a)) and has an "output electrode from which an output signal of the semiconductor apparatus is output." A power conditioner does not anticipate an active device.

(2) As there is no disclosed signal line, there can be no "gate electrode connected to a signal line" as is recited in claim 32.

(3) One of the Applicant's gates in claim 32 is coupled to a signal line (the output transistor), as noted above, and the other is connected to a ground voltage terminal (the protection transistor). Sugerman's gates are not so connected. They are connected to one another and both are connected to the source of the trigger transistor, contrary to the Applicant's recitation that the other gate is connected to ground. *Neither* of Sugerman's gates is connected to ground (if 30 is taken as a ground, for argument's sake[1]); they are both connected to a resistor R10, which is not at ground voltage as the applicant claims. (The drain is 190 and the source is 200 in Fig. 5 of Sugerman (col. 6, line 41), so the source is coupled to bus bar 30.)[2]

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[1] Sugerman says that neither 20 or 30 is a ground, but are interchangeably "high potential" and "low potential" (col. 5, lines 38-42).

[2] The Applicant previously argued: "The Examiner is invited to note that the Applicant's Fig. 1(a) differs from Sugerman's Fig. 4 in showing the two transistors being similarly oriented, while in Sugerman's Fig. 4 the transistors are oriented as in mirror images. This means that in Sugerman's drawing there is no direct path from the gate of the protection resistor M11 to the gate of the output transistor M10, while the Applicant's Fig. 1(a) shows the gate 14 of protection transistor 10 being directly coupled to the P-well 27 of the output transistor 11. The Applicant's specification notes this: "A gate electrode 14 of the NMOS dummy transistor 10 is connected to the P-well 22 via the P+ contact layer

(4) As Sugerman does not disclose a device with an input and an output, Sugerman does not disclose the claimed "output" transistor. It discloses two protection transistors, one of which is called a "trigger" transistor and serves as an adjunct to the main "protection" transistor (Abstract and elsewhere).

(5) With respect, Sugerman lacks the claimed second-conductivity-type layer located under the gate electrode of the output transistor. Referring to Fig. 5, Sugerman's region 110 is P, 120 is N, and regions 130/140 are P-wells; one is isolated from substrate 110, the other is shorted to it (col. 6, lines 17-26). The Examiner refers to region 210[3] as a second-conductivity-type layer, but 210 (also a "Pwell," see col. 7, line 4) is neither located under a gate electrode (since 160 is the trigger gate, see col. 6,line 33) nor is it connected to a gate by metal wiring.[4]

(6) The claimed metallic wiring connects the second-conductivity-type layer to the gate of the protection resistor. If region 210 (or,140) is the second-conductivity-type layer, as the Examiner asserts (not admitted), then it is confined to one transistor and cannot meet this claim language.

[3-4] Claims 2, 3, and 6-15 were rejected under §103(a) as being unpatentable over Sugerman in view of Staab '790. This rejection is respectfully traversed on the basis of the arguments above for claim 1, from which those claims depend.

[5] Claims 16-30 remain allowed.

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27 of the NMOS output transistor 11" (page 10, line 13). The connection is made via the electrode wiring 28, which is now labeled in Figs. 1(b) and 2.

[3] Region 140 is also said to anticipate this feature, at page 3, line 5. Clarification is requested.

[4] The Applicant previously argued: "Fig. 5 shows ... the resistor being connected to gates 170 and 160 (also shown in Fig. 4, as mentioned above) and contacts 220, both of which are adjacent to the P Well 140. However, these contacts 220 are not in direct contact with the P Well 140 and therefore they are not "connected" to the PWell 140. What they *are* connected to is the source 200 (col. 6, line 41) and a "bulk region" 210 (col. 6, line 46) which is identical in appearance to the source 200 and drain 190. Thus, the gate is not "*connected by an electrode wiring to said second-conductivity-type layer* [140] *under the gate* [160] *of said first-conductivity-type MOS output transistor* [M10]" as claimed, and there is no anticipation of this feature. The word "connected" implies that there is nothing intermediate. New claim 31 makes this feature more explicit by reciting that the connection of claim 1 is 'direct.'"

Withdrawal of the rejections, and allowance of the remaining claims, is requested.

The Examiner apparently has not examined claim 31. An Action including examination of claim 31 is requested.

Respectfully submitted,

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Date

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